AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1(currently amended). A cache memory, comprising:

a flag holding unit which holds, in a correspondence with a cache entry ~~which~~ that holds a data unit of caching, a valid flag indicating whether or not the cache entry is valid, and a dirty flag indicating whether or not the cache entry has been written into;

a command holding unit which is configured of a register that allows access from a processor by a data transfer instruction, and holds a command issued by [[a]] the processor by a data transfer instruction; and

an altering unit operable to alter, based on a command held by said command holding unit, at least one of the valid flag and the dirty flag, contrary to the state of the cache entry, wherein the command to said command holding unit is issued by a data transfer instruction, the command being data transferred by the data transfer instruction, said altering unit operating independently of an operation of the processor, and performs the altering while the cache memory is not accessed by the processor.

2 (currently amended). The cache memory ~~according to Claim~~ of claim 1,

wherein said altering unit is operable to set, in the cache entry, an address serving as a tag, and to set the valid flag, without loading data from a memory.

3 (currently amended). The cache memory ~~according to Claim~~ of claim 2,

wherein said altering unit is operable to reset the dirty flag of the cache entry in a state in which the cache entry holds rewritten data that has not been written back.

4 (currently amended). The cache memory ~~according to Claim~~ of claim 2, further comprising:

a holding unit which holds an address range specified by the processor; and

an identification unit operable to identify a cache entry which holds data belonging to the held address range,

wherein said altering unit is operable to alter at least one of the valid flag and the dirty flag of the identified cache entry.

5 (currently amended). The cache memory ~~according to Claim~~ of claim 4,

wherein said identification unit includes:

a first conversion unit operable, in the case where a start address of the address range indicates a point midway through line data, to convert the start address into a start line address indicating a start line included in the address range;

a second conversion unit operable, in the case where an end address of the address range indicates a point midway through the line data, to convert the end address into an end line address indicating an end line included in the address range; and

a judgment unit operable to judge whether or not there exist cache entries which hold data corresponding to respective line addresses from the start line address to the end line address.

6 (currently amended). The cache memory ~~according to Claim~~ of claim 1, wherein said altering unit further includes:

an instruction detection unit operable to detect execution of a memory access instruction having a dirty flag reset directive; and

a flag rewriting unit operable to reset a dirty flag of a cache entry which is accessed according to the instruction.

7 (currently amended). The cache memory ~~according to Claim~~ of claim 1, wherein said altering unit further includes:

an instruction detection unit operable to detect execution of a memory access instruction having a valid flag reset directive; and

a flag rewriting unit operable to reset a valid flag of a cache entry which is accessed according to the instruction.

8 (currently amended). A method for controlling a cache memory having, in a correspondence with a cache entry which holds a data unit of caching, a valid flag indicating whether or not the cache entry is valid, and a dirty flag indicating whether or not the cache entry has been written into, the cache entry holding a data unit of caching, ~~said~~ the method comprising:

causing a predetermined register to hold a ~~holding step of holding a~~ command issued by a processor, the processor executing a data transfer instruction that transfers data as the command to the predetermined register;

~~a step of~~ setting, in the cache entry, an address serving as a tag, and setting the valid flag, without loading data from a memory, based on a held command; and

~~a step of~~ resetting, based on a held command, the dirty flag of the cache entry in a state in which the cache entry holds rewritten data that has not been written back, wherein setting the valid flag and resetting the dirty flag are performed independently of an operation of the processor, and are performed while the cache memory is not accessed by the processor.

9 (currently amended). The cache memory ~~according to Claim~~ of claim 3, further comprising:

a holding unit which holds an address range specified by the processor; and

an identification unit operable to identify a cache entry which holds data belonging to the held address range,

wherein said altering unit is operable to alter at least one of the valid flag and the dirty flag of the identified cache entry.

10 (currently amended). The cache memory ~~according to Claim~~ of claim 9,

wherein said identification unit includes:

a first conversion unit operable, in the case where a start address of the address range indicates a point midway through line data, to convert the start address into a start line address indicating a start line included in the address range;

a second conversion unit operable, in the case where an end address of the address range indicates a point midway through the line data, to convert the end address into an end line address indicating an end line included in the address range; and

a judgment unit operable to judge whether or not there exist cache entries which hold data corresponding to respective line addresses from the start line address to the end line address.

11 (new). The cache memory of claim 1, wherein said command holding unit includes a first field that specifies an operation to the valid flag, and a second field that specifies an operation to the dirty flag.